Amendments to the Claims

List of claims:

Claims 1 - 23 (Cancelled).

24. (Previously presented) The signal level displacement circuit as claimed in claim 27, wherein the circuit node is arranged to discharge in the evaluation phase in response to the data signal being logically high and the circuit node is arranged to not discharge in the evaluation phase in response to the data signal being logically low.

25 (Cancelled).

26. (Cancelled).

27. (Currently amended) A signal level displacement circuit for a flip flop operable to be clocked by a clock signal, the signal level displacement circuit comprising:

a signal delay circuit configured to generate a delayed clock signal corresponding to the clock signal delayed by a time delay;

a programmable capacitor unit coupling a circuit node to a reference potential, the programmable capacitor unit arranged to charge to an operating voltage in a charging phase in response to the clock signal being logically low and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed and inverted clock signal being logically high, the programmable capacitor network having a programmable capacitance;

a first isolating circuit configured to be clocked by the clock signal and having an input connected to the circuit node;

a second isolating circuit configured and arranged to be clocked by the delayed clock signal;

wherein an output of the first isolating circuit feeds back to the input of the first isolating circuit via the second isolating circuit; and

a slave latch circuit;

wherein the first isolating circuit has an output connected to the slave latch circuit, the first isolating circuit is configured to generate an output signal at the output, and the slave latch circuit is configured to buffer-store the output signal; and

wherein the first isolating circuit and the second isolating circuit are located outside the slave latch circuit.

28. (Previously presented) The signal level displacement circuit as claimed in claim 27, wherein the signal delay circuit, the circuit node, and the programmable capacitor network are incorporated into a master latch circuit.

29. (Previously presented) The signal level displacement circuit as claimed in claim 28, wherein:

the master latch circuit further includes an inverter configured to generate an inverted clock signal corresponding to an inversion of the clock signal;

the master latch circuit further includes a first controllable switch driven by the inverted clock signal; and

the first controllable switch switches the operating voltage to the circuit node in response to the clock signal being logically low.

30. (Previously presented) The signal level displacement circuit as claimed in claim 28, wherein:

the master latch circuit further includes a reference potential node configured to be coupled to a reference potential;

the master latch circuit further includes a second, third and fourth controllable switches, the second, third and fourth controllable switches being connected in series with one another between a voltage supply and the reference potential node.

31. (Previously presented) The signal level displacement circuit as claimed in claim 30, wherein the master latch circuit is configured to generate a delayed inverted clock signal and to drive the second controllable switch with the delayed inverted clock signal.

32. (Previously presented) The signal level displacement circuit as claimed in claim 30, wherein the third controllable switch is arranged to be driven by the data signal.

33. (Previously presented) The signal level displacement circuit as claimed in claim 30, wherein the fourth controllable switch is arranged to be driven by the clock signal.

34. (Previously presented) The signal level displacement circuit as claimed in claim 30, wherein the capacitor is connected in parallel with the second, third and fourth controllable switches.

35. (Previously presented) A signal level displacement circuit for a flip flop operable to be clocked by a clock signal, the signal level displacement circuit comprising:

a signal delay circuit configured to generate a delayed clock signal corresponding to the clock signal delayed by a time delay;

a programmable capacitor network coupling a circuit node to a reference potential, the programmable capacitor network arranged to charge to an operating voltage in a charging phase in response to the clock signal being logically low and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed and inverted clock signal being logically high, the programmable capacitor network having a programmable capacitance;

wherein the signal delay circuit, the circuit node, and the programmable capacitor network are incorporated into a master latch circuit; and

wherein the time delay is adjustable.

36. (Previously presented) A signal level displacement circuit for a flip flop operable to be clocked by a clock signal, the signal level displacement circuit comprising:

a signal delay circuit configured to generate a delayed clock signal corresponding to the clock signal delayed by a time delay;

a programmable capacitor network coupling a circuit node to a reference potential, the programmable capacitor network arranged to charge to an operating voltage in a charging phase in response to the clock signal being logically low and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed and inverted clock signal being logically high, the programmable capacitor network having a programmable capacitance;

wherein the signal delay circuit, the circuit node, and the programmable capacitor network are incorporated into a master latch circuit; and wherein during the evaluation phase the capacitor discharges with a time constant in response to the data signal being logically high and the time constant is less than the time delay.

37. (Previously presented) The signal level displacement circuit as claimed in claim 28, wherein the master latch circuit is configured to make the time delay is less than a time period of the clock signal.

38. (Previously presented) The signal level displacement circuit as claimed in claim 28, wherein the signal delay circuit comprises a plurality of inverter stages connected in series.

39. (Previously presented) The signal level displacement circuit as claimed in claim 28, wherein the master latch circuit is configured to receive only a single supply voltage.

Claims 40 - 42 (Cancelled).